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Clean Version of Pending Claims

DUAL-STAGE COMPARATOR UNIT
Applicant: James E. Jaussi et al.
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1. (Amended) A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes, a switch connected across the pair of output nodes, and a non-linear load connected across the pair of output nodes; and

a second amplifier stage coupled to the pair of output nodes, the second amplifier stage including an input pair of isolated gate field-effect transistors and a cross-coupled pair of isolated gate field-effect transistors, wherein each of the cross-coupled pair of isolated gate field-effect transistors is coupled in parallel with a corresponding one of the input pair of isolated gate field-effect transistors.

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2. The comparator unit of claim 1, wherein the differential amplifier comprises a pair of differential pairs of isolated gate field-effect transistors.

3. The comparator unit of claim 2, wherein the switch comprises an electronically controllable switch.

4. The comparator unit of claim 3, wherein the electronically controllable switch comprises an isolated gate field-effect transistor.

5. The comparator unit of claim 4, wherein the non-linear load comprises a pair of cross-coupled isolated gate field-effect transistors.

6. The comparator unit of claim 5, wherein each transistor in the pair of cross-coupled isolated gate field-effect transistors comprises an *n*-channel isolated gate field-effect transistor.

7. The comparator unit of claim 1, wherein the second amplifier stage comprises a non-linear amplifier.

8. (Amended) The comparator unit of claim 7, wherein the second amplifier stage includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes.

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9. The comparator unit of claim 1, wherein the differential amplifier comprises a differential pair of isolated gate field-effect transistors.

10. A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes including a first output node and a second output node, a non-linear load connected across the pair of output nodes, and a first switch connected between the first output node and a common node and a second switch connected between the second output node and the common node; and

a second amplifier stage coupled to the pair of output nodes.

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11. The comparator unit of claim 10, wherein the differential amplifier comprises a pair of differential pairs of isolated gate field-effect transistors.

12. (Amended) The comparator unit of claim 11, wherein the first switch comprises an optically controllable switch.

13. The comparator unit of claim 12, wherein the optically controllable switch comprises a photo-transistor.

14. The comparator unit of claim 13, wherein the non-linear load comprises a pair of cross-coupled bipolar transistors.

15. The comparator unit of claim 14, wherein the second amplifier stage comprises a non-linear amplifier.

16. The comparator unit of claim 15, wherein the non-linear amplifier includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes.

17. The comparator unit of 16, wherein the non-linear amplifier includes a pair of cross-coupled *p*-channel isolated gate field-effect transistors connected across the pair of second stage output nodes, a non-linear load connected across the pair of second stage output nodes, and a pair of input transistors connected across the non-linear load.

18. A signal transmission unit comprising:

a differential signal source;

a comparator unit comprising:

a first amplifier stage including a pair of differential amplifiers having a pair of input nodes and a pair of output nodes, a switch connected across the pair of output nodes, and a non-linear load connected across the pair of output nodes; and

a second amplifier stage coupled to the pair of output nodes; and

a transmission line to couple the differential signal source to the comparator unit.

19. The signal transmission unit of claim 18, wherein the differential signal source is formed on a first integrated circuit die, the comparator unit is formed on a second integrated circuit die, and the transmission line is formed on a substrate on which the first integrated circuit die and the second integrated circuit die are mounted.

20. The signal transmission unit of claim 19, wherein the second integrated circuit die comprises a processor.

21. The signal transmission unit of claim 20, wherein the first integrated circuit die comprises a communication unit.

22. The signal transmission unit of claim 20, wherein the first integrated circuit die comprises a data storage unit.

23. The signal transmission unit of claim 20, wherein the first integrated circuit die comprises an amplifier.

24. A method of processing a differential signal, the method comprising:

beginning an equalization phase in a first amplifier stage;

beginning an equalization phase in a second amplifier stage about one gate delay after beginning the equalization phase in the first amplifier stage;

evaluating the differential signal in the first amplifier stage to form a first stage output differential signal after completing the equalization phase in the first amplifier stage; and

evaluating the first stage output differential signal in the second amplifier stage after completing the equalization phase in the second amplifier stage.

25. The method of claim 24, wherein beginning an equalization phase in a first amplifier stage comprises:

closing a switch in the first amplifier stage.

26. The method of claim 24, wherein beginning an equalization phase in a first amplifier stage comprises:

closing a plurality of switches in the first amplifier stage.

27. The method of claim 26, wherein evaluating the differential signal in the first amplifier stage to form a first stage output differential signal after completing the equalization phase in the first amplifier stage comprises:

applying linear amplification to the differential signal to form an amplified differential signal; and

applying non-linear amplification to the amplified differential signal to form the first stage output differential signal.

28. The method of claim 27, wherein evaluating the first stage output differential signal in the second amplifier stage after completing the equalization phase in the second amplifier stage comprises:

applying non-linear amplification to the first stage output signal.

29. A comparator unit comprising:

a first amplifier stage including a differential amplifier having a pair of input nodes and a pair of output nodes including a first output node and a second output node, a non-linear load connected across the pair of output nodes, and a first switch connected between the first output node and a common node, a second switch connected between the second output node and the common node, and a third switch connected between the first output node and the second output node; and

a second amplifier stage coupled to the pair of output nodes.

30. The comparator unit of claim 29, wherein the third switch comprises an electronically controllable switch.

31. The comparator unit of claim 30, wherein the electronically controllable switch comprises an isolated gate field-effect transistor.

32. The comparator unit of claim 29, wherein the non-linear load comprises a pair of cross-coupled isolated gate field-effect transistors.

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33. The comparator unit of claim 29, wherein the second amplifier stage comprises a non-linear amplifier.

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34. The comparator unit of claim 29, wherein the second amplifier stage includes a pair of second stage output nodes and a switch connected across the pair of second stage output nodes.